REMARKS

Applicant respectfully requests further examination and reconsideration in view of the above claim amendments and arguments set forth below. Claims 1, 2, 9-12, 16-17, 20-21, and 25-26 are rejected under 35 U.S.C. 102 (e). Claims 3-8, 13-15, 18-19, 22-24, 27 and 28 are rejected under 35 U.S.C. 103 (a). The Abstract has herein been amended. Claims 1, 11, and 20 have herein been amended. All amendments are supported by the specification. No new matter has been added as a result of this amendment. Therefore, Claims 1-28 remain pending in the case.

Objection to the Abstract

The Abstract is objected to because it is not in proper abstract language and format under MPEP section 608.01(b). The Abstract is herein amended to overcome the objection.

35 U.S.C. § 102 rejections

Claims 1, 2, 9-12, 16-17, 20-21, and 25-26 have are rejected under 35 U.S.C. 102 (e) as being anticipated by US patent 6,173,381 (Dye).

Independent Claims 1, 11, and 20

Dye discloses a memory controller with improved performance because it includes data compression and decompression engines. The improved performance is apparently the result of reduced system bottlenecks resulting from data compression. The compressed data requires less bandwidth for transmission over the system bus (see *inter alia*, the Abstract and col.2, line 25- col. 3, line 59). In figure 5 of Dye, an integrated memory controller (IMC) is shown, coupled to other systems through FIFO buffers 204, 206, 214 and 216. The rejection claims that the FIFO's 204, 206, 214 and 216 are equivalent to the storage element taught

and claimed by the present invention. Applicant respectfully traverses this proposition. The FIFO's 204, 206, 214 and 216 are functioning as decoupling points necessary to transfer data in and out of the synchronous IMC to other parts of the system, operating in an asynchronous mode. However, nowhere does Dye disclose a storage element that is separate from a memory but combinable with it to form a buffer for CPU instructions that has an effective size equal to the size of the entire buffer and graphics memory combined. Dye further fails to teach a storage element being controlled by an engine (claim 1), memory controller (claim 11) or a graphics memory controller (claim 20), wherein the engine or controller receives commands from the CPU via an interface and uses the storage element to store the received commands, as claimed. The present invention discloses and claims an engine or controller that is operative to receive commands from a CPU, store the commands in a storage element. In one embodiment, the engine or controller is coupled to the storage element via an internal interface. The engine or controller may in some cases incorporate (combine) a graphic memory with the storage element to act as a single buffer memory from the perspective of the CPU. This engine or controller further relieves the CPU from the management of the storage element and the memory. However incorporate, nowhere does Dye disclose an engine, a memory controller or a graphics engine that can "utilize the graphics memory as well as a storage element ... as the buffer for CPU purposes," where the "effective size of the entire buffer can be virtually the size of the graphics memory" (page 8, lines 16-21). Claims 1, 11, and 20 have been amended to include the limitation of "wherein the engine incorporates the memory as part of the storage" (see page 4, line 1).

Because not every element of Claims 1, 11 and 20 (as amended) are taught by the reference, the 102(e) rejection is unsupported by the art. Therefore, Applicant respectfully requests the withdrawal of the 102 (e) rejection of Claims 1, 11, and 20 and the allowance of the claims.

Dependent Claims 2, 9-10, 16-17, 21, and 25-26

Claims 2, 9-10, 16-17, 21, and 25-26 are dependent claims of Claims 1, 11, and 20, respectively. As such, Claims 2, 9-10, 16-17, 21, and 25-26 are patentable for at least the same reasons as Claims 1, 11 and 20.

35 U.S.C. § 103 rejections

Claims 3-8, 13-15, 18-19, 22-24, 27 and 28

Claims 3-8, 13-15, 18-19, 22-24, 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dye as applied to claims 1, 2, 9-12, 16-17, 20-21, and 25-26.

Claims 3-8, 13-15, 18-19, 22-24, 27 and 28 are dependent claims of Claims 1, 11, and 20, respectively. As such, Claims 2, 9-10, 16-17, 21, and 25-26 are patentable for at least the same reasons as Claims 1, 11 and 20.

Additionally, Dye fails to disclose a method or system as claimed in Claim 6 and 26, where the "effective size of the buffer as viewed by the CPU can be as large as the memory." As previously discussed, nowhere does teach or suggest a method or system combining a storage element with a memory to form a larger virtual buffer, under the control of a graphic controller or engine, and used for receiving CPU commands. Dye fails to teach or suggest any combination of any type of storage element, be it a circular FIFO, a double FIFO or a triple FIFO with a memory to form a larger virtual buffer for receiving CPU commands. Therefore, Applicants respectfully assert that Claims 3-8, 13-15, 18-19, 22-24, 27 and 28 are patentable over the Dye for at least the reasons stated above.

Conclusion

For these reasons discussed above, Applicant respectfully submits that Claims 1-28 are now in condition for allowance and such action is earnestly solicited by Applicant.

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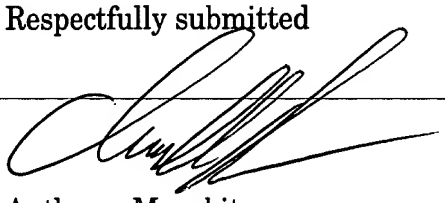
Respectfully submitted



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